REMARKS

This Amendment is responsive to the Office Action dated April 18, 2006. All objections and rejections of the Examiner are respectfully traversed. Reconsideration and further examination are respectfully requested.

Applicants wish to thank Examiner Siddiqi for his generosity in providing a telephone interview regarding this application with the undersigned Attorney on July 10, 2006. While no agreement regarding the rejections in the Office Action was reached during that discussion, the Examiner's explanations regarding the rejections are considered to be very helpful, and the contents of this paper are intended to reflect those explanations.

At paragraph 3 of the Office Action, the Examiner rejected claims 1, 12 and 23 for being non-statutory subject matter under 35 U.S.C. 101. Applicants respectfully traverse this rejection.

While paragraph 3 of the Office Action indicates claim 11, the Examiner clarified in the telephone interview that independent claim 12 was the intended claim in this rejection. Accordingly, the following remarks address independent claims 1, 12 and 23.

The Court of Appeals for the Federal Circuit has held that a claimed invention as a whole must produce a "useful, concrete and tangible result." State Street Bank & Trust v. Signature Financial Group Inc., 149 F. 3d 1369 at 1373-74, 47 USPQ2d 1569 (Fed. Cir. 1998) at 1601-02. Each of the present independent claims 1, 12 and 23, recite a "packet count" and a "byte count", as well as "reading" and "storing" the "packet count" and "byte count" in a "single memory location of [a] memory device". As it is generally known, packet counts and byte counts are useful in managing communication devices and/or end stations connected to a communication network. Additionally, the "single memory location of [a] memory device" in which the packet

count and byte count are maintained by the independent claims 1, 12 and 23 indicates that the packet and byte counts in those claims are both concrete and tangible. Those skilled in the art will recognize that the "memory device" of the independent claims 1, 12 and 23 refers to a tangible hardware entity that is an internal data storage component of an electronic device.

Applicants respectfully disagree with the Examiner's assertion that the claims raise a question as to whether they "are directed merely to an abstract idea that is not tied to a technological art". A person skilled in the art, upon reading independent claims 1, 12 and 23, as well as the accompanying Detailed Description as originally filed, would recognize that the present invention falls within the computer-related technological arts. This is apparent from the language of the claims (e.g. "memory location of the memory device", "storing the entire set of bits", "receiving at least one data packet", etc.), as well as the teachings in the Detailed Description (e.g. Fig. 16 and related discussion on pages 19-20, etc.). Moreover, a person skilled in the art, upon reading the independent claims 1, 12 and 23, would recognize that the "single memory location of the memory device" is a physical object that is transformed into a different state in these claims. The transformation is accomplished through the "reading", "determining" and "storing" performed with regard to the "single memory location".

For the above reasons Applicants respectfully submit that the present independent claims 1, 12 and 23 are statutory subject matter under 35 U.S.C. 101.

Applicants also note that this is the first time that an issue under 35 U.S.C. 101 has been raised during the prosecution of this application, which dates back almost six years to its filing on December 22, 2000. Nothing in the four previously issued Office Actions, which were rejections based on prior art, as well as the two Advisory Actions indicating the necessity of further searching, raised any issue with regard to whether the subject matter of claims 1, 12, and

23, either as they were initially filed or subsequently amended, was statutory under 35 USC 101. The Examiner has cited no precipitating event or change of circumstances that caused the introduction of this new grounds of rejection. In particular, the Examiner has cited no substantive legal development, such as a court decision, that would result in a change in how claims 1, 12 and 23 should be treated in terms of protectability. Neither has the Examiner indicated any amendment by Applicants that changed these claims in a way that would require this new ground of rejection. Applicants respectfully urge that no such change of law or amendment has occurred, and that the present claims 1, 12 and 23 are currently statutory subject matter under 35 U.S.C. 101, and have been directed to statutory subject matter since they were originally filed on December 22, 2000.

In paragraphs 4-5 of the Office Action, the Examiner rejected claims 8, 19 and 30 under 35 USC 112, first paragraph, for not complying with the written description requirement. Applicants respectfully traverse this rejection.

Applicants respectfully direct the Examiner's attention to the specification as originally filed beginning at line 14 on page 20, which states as follows:

> If the 32-bit value is negative, meaning bit 31 is high, the 36-bit addition may be performed on the Data[35:0] field. . .

Applicants respectfully urge that the above cited text meets the written description requirement for the present claims 8, 19 and 30. As these claims are unchanged since the original filing of the application, Applicants further respectfully urge that the written description requirement has similarly been met by these claims since the original filing of the application.

In paragraphs 6-7 of the Office Action, the Examiner rejected claims 8, 19 and 30 for lack of antecedent basis for the term "the value". Claim 8 depends claim 7, claim 19 depends from claim 18, and claim 30 depends from claim 29. Each of claims 7, 18 and 29 include antecedent basis for the cited term "a value". Applicants respectfully urge that the term "a value" in each of claims 7, 18 and 29 provides sufficient antecedent basis for the term "the value" in claims 8, 19 and 30. Accordingly, the requirements of 35 USC 112, second paragraph are met with regard to the dependent claims 8, 19 and 30. As these claims are unchanged since the original filing of the application, Applicants also respectfully urge that antecedent basis for "the value" in claims 8, 19 and 30 has been met by the term "a term" in the parent claims 7, 18 and 29 since the original filing of the application.

In paragraphs 8-35 of the Office Action, the Examiner rejected claims 1-9, 11-20, 22-31, and 33-39 for anticipation under 35 USC 102(b), citing United States patent 5,231,593 ("Notess"). Applicants respectfully traverse this rejection.

Notess discloses a system for collecting and displaying statistical data for a plurality of local area networks (LANs). The data is collected by several remote nodes in the Notess system, and is obtained by using a LAN driver that intercepts all records on the LAN. The records are sent to a collector process where statistics are accumulated into a shared memory area and then transferred to an archiver process in a management node. The Notess archiver process writes the statistics to a history file while compressing older data to prevent the file from growing too large.

Beginning at line 38 of column 5, Notess teaches waiting until a buffer of data is available from the LAN driver, and then reading the buffer and processing the packets of data in the buffer and assembling the statistics. This process continues to process available buffers until

the collector process is canceled by the user of the Notess system. The collector process of Notess does not terminate by itself, but must be canceled by the user of the system.

The shared memory of Notess contains a counter for the total number of packets transmitted across the LAN, and also a counter for the total number of bytes from all the packets. The Notess collector process may maintain separate counters for packets having lengths within certain ranges.

Nowhere in Notess is there disclosed or suggested any method or system for monitoring a network, including:

> receiving at least one data packet;
> reading an entry of a memory device, the entry of the memory device containing both a first statistical value and a second statistical value, ***wherein the entry is a single memory location of the memory device, wherein the first statistical value includes a packet count, and wherein the second statistical value includes a byte count***;
> determining a third statistical value based on at least one of a content of the at least one data packet, the first statistical value, and the second statistical value, wherein the third statistical value includes a new value of the packet count and a new value of the byte count;
> storing the entire set of bits of the determined third statistical value into the entry of the memory device; and
> ***wherein said reading, determining and storing are performed without interruption***. (emphasis added)

As in the present independent claim 1. Independent claims 12 and 23 recite analogous features. Nothing in Notess provides any hint or suggestion of even the desirability of storing both a packet count and a byte count in a single location within a single memory location of a memory device, nor of reading the memory location, determining new values for the counters, and writing the memory location without interruption, as in the present independent claims 1, 12 and 23. In contrast to storing packet count and byte count in a single memory location, Notess teaches storing a packet count and a byte count in a *shared memory*. As shown in Fig. 1 of

Notess, the Notess shared memory 108 is shared among multiple software processes, labeled the Collector 106 and the Agent 110. A person skilled in the art would recognize that a memory shared across multiple software processes, as in Notess, is far different from a single memory location that stores multiple counters, as in the present independent claims. Applicants respectfully urge that the meaning of "single memory location" is plain on its face, and that its meaning in this context is re-enforced and confirmed by the teachings beginning at line 6 on page 20 of the Specification as originally filed. Moreover, Notess includes no teaching of any specific number of memory locations that may be used to store the byte counters and/or the packet counters it maintains.

Notess also includes no teaching or suggestion of reading, determining new values, and writing of the byte counters and/or packet counters without interruption, as in the present independent claims 1, 12 and 23. In clear contradistinction, Notess teaches a collector process that sets up a series of interrupt handlers in block 406 of Fig. 4, which would be triggered by interrupts "that would occur while it is collecting data". Notess further describes a separate archiver process that copies the collected statistics from the shared memory to an archiver process in a management node (see Notess Fig. 6). The Notess archiver process sets up a signal handler in step 710 of Fig. 7 and *a periodic interrupt* that triggers the steps shown in Fig. 8. Nothing in the Notess description of actions performed by the collector process of Figs. 4 and 5 to handle interrupts with signal handlers during statistics collection, nor in the description of the actions of setting up and handling of interrupts performed by the archiver process shown in Figs. 7 and 8 to archive statistics, nor in the description of actions performed by the agent process shown in Fig. 6 to return statistics to the archiver process, discloses or suggests the steps of reading, determining and storing packet and byte counters both located in a single memory

location without interruption, as in the present independent claims 1, 12 and 23. Instead, Notess anticipates and provides for setting up, receiving and processing interrupts throughout the collecting, returning and archiving of the statistics it maintains.

For the above reasons, Applicants respectfully urge that Notess does not disclose or suggest all the features of the present independent claims 1, 12 and 23. Notess therefore does not anticipate the present independent claims 1, 12 and 23 under 35 U.S.C. 102. As claims 2-9, 11, 13-20, 22, 24-31, and 33-39 each depend either directly or indirectly from claims 1, 12, and 23, they are respectfully believed to be patentable over Notess for at least the same reasons.

In paragraphs 36-37 of the Office Action, the Examiner rejected claims 10, 21 and 32 as being obvious under 35 U.S.C. 103, citing Notess in combination with United States patent number 4,187,080 of Soha ("Soha"). Applicants respectfully traverse this rejection.

Nowhere in the combination of Notess and Soha is there disclosed or suggested any method or system for monitoring a network, including:

> receiving at least one data packet;
>
> reading an entry of a memory device, the entry of the memory device containing both a first statistical value and a second statistical value, ***wherein the entry is a single memory location of the memory device, wherein the first statistical value includes a packet count, and wherein the second statistical value includes a byte count***;
>
> determining a third statistical value based on at least one of a content of the at least one data packet, the first statistical value, and the second statistical value, wherein the third statistical value includes a new value of the packet count and a new value of the byte count;
>
> storing the entire set of bits of the determined third statistical value into the entry of the memory device; and
>
> ***wherein said reading, determining and storing are performed without interruption***. (emphasis added)

As in the present independent claims 1, 12 and 23. Soha expressly describes a system in which packet and byte counters are stored in separate memory locations, and in which the packet and byte counters are updated in separate, independent operations. As stated in Soha at column 6 in lines 55 - 69, the microprocessor operates in response to a received packet by "by fetching the contents of ***a predetermined location in the packet memory 50 that serves as a packet counter***, incrementing those contents, and writing them back into that location" (emphasis added). This section describes clearly that, as shown in step 58 of Fig. 5, the Soha system uses a first memory entry ("a predetermined location") located within the counter section of packet memory 50 to store a packet counter. The operation of the Soha system at step 58 is solely related to updating the packet counter stored at that memory location within the counter section of the packet memory 50. In this way Soha expressly teaches a first independent step of writing a new value to a packet counter that is performed prior to further processing of the received packet, including the determination of a new byte count value to be used to write to a separate byte counter.

In a separate, independent step 62 shown in Fig. 5 in Soha, a second, subsequent operation is performed after the writing of the packet count in step 58. In this separate step, the Soha microprocessor fetches a count of the number of bytes in the received packet, and writes a new value to another location within the packet memory 50 that is used as a counter for a byte counter. This is confirmed in column 7 lines 10-14 of Soha, which states that the "microprocessor fetches the contents of ***that location***, adds to them the packet byte count that it fetched from the packet-storage part of the packet memory 50, and ***returns the results to that location***" (emphasis added). The above cited sections of Soha expressly teach the maintenance of two separate memory locations within the packet memory 50, that are used to separately store packet and byte counters, and that are updated in separate, independent steps.

That the packet and byte counters of Soha are independently stored in two separate memory locations through two independent steps is further taught at line 15 of column 7, which states:

> In both of the ***operations*** represented by levels 58 and 62, the location of the counter to be updated was predetermined; the program memory 53 contains the ***locations*** of the ***packet and byte counters***, so the microprocessor does not have to employ the look-up engine 54 and the look-up table 56 in order to locate the counter of interest. (emphasis added)

Thus it is clear that the packet and byte counters of Soha consist of separate memory locations that are updated and stored in separate, independent operations upon receipt of a packet.

These deficiencies of Soha with regard to the above indicated features of the present independent claims 1, 12 and 23 are not remedied by the teachings of Notess, which are discussed in detail above with reference to the rejections under 35 USC 102.

For the above reasons, Applicants respectfully urge that the combination of Notess and Soha fails to disclose or suggest all the features of the present independent claims 1, 12 and 23, from which claims 10, 21 and 32 depend. Accordingly, the combination of Notess and Soha. does not support a *prima facie* case of obviousness with regard to the present independent claims 1, 12 and 23 under 35 U.S.C. 103. As to claims 10, 21 and 32, they each depend either directly or indirectly from independent claims 1, 12 and 23, and are respectfully believed to be patentable over the combination of Notess and Soha for at least the same reasons. Reconsideration of all pending claims is respectfully requested.

In view of the above, Applicants respectfully urge that the present claims are allowable, and respectfully request that all rejections of the Office Action be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone David A. Dagg, Applicants' Attorney at 617-630-1131 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

/David Dagg/
David A. Dagg Reg. No. 37,809
Attorney/Agent for Applicant(s)
McGuinness & Manaras LLP
125 Nagog Park Drive
Acton, MA 01720
(617) 630-1131

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